



Docket No. 303.145US3  
WD # 349772

Micron Ref. No. 95-1086.03

**Clean Version of Pending Claims**

**CIRCUIT AND METHOD FOR MEASURING AND FORCING AN INTERNAL VOLTAGE  
OF AN INTEGRATED CIRCUIT**

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Serial No.: 09/633,375

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*Claims 19-73, as of January 23, 2003 (Date of Response to Second Office Action filed).*

19. A method for measuring a voltage at an internal node of an integrated circuit, the method comprising:

coupling a pass circuit between the internal node and a pin of the integrated circuit;  
using a reset circuit to activate the pass circuit; and  
driving the pass circuit to pass the voltage from the internal node to the pin.

20. The method of claim 19, further comprising using a pass control circuit to drive the pass circuit.

21. The method of claim 20, further comprising using the pass control circuit to provide at least one output signal to selectively drive the pass circuit to pass a voltage from the internal node to the pin, thereby allowing the voltage at the internal node to be read after the integrated circuit is packaged.

22. The method of claim 20, wherein the pass control circuit comprises an n-channel MOS transistor having a drain coupled to the internal node, the n-channel MOS transistor configured to, when turned on, pass the voltage at the internal node to a source of the n-channel MOS transistor and to the pass circuit.

23. The method of claim 19, further comprising providing an oscillating control signal to the pass circuit.

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Sub E1*
24. The method of claim 23, further comprising using a ring oscillator to provide the oscillating control signal to the pass circuit.
25. The method of claim 19, further comprising using a pass control circuit to apply a desired voltage to the internal node, thereby forcing the voltage at the internal node to the desired voltage.
26. The method of claim 19, wherein the pass circuit comprises:  
a pass gate having first, second, and third terminals, the first terminal coupled to a pass control circuit, the second terminal coupled to the internal node, the third terminal coupled to the pin; and  
a capacitor coupled between the first terminal of the pass gate and the pass control circuit such that a voltage at the first terminal of the pass gate is driven to cause a voltage at the second terminal voltage to be passed to the third terminal for reading the voltage at the internal node.
- B1*
27. The method of claim 26, wherein the pass gate comprises an n-channel MOS transistor.
28. A method for forcing a voltage at an internal node of an integrated circuit to a desired level, the method comprising:  
coupling a pass circuit between the internal node and a pin of the integrated circuit;  
applying a voltage of the desired level to the pin;  
using a reset circuit to activate the pass circuit; and  
driving the pass circuit to pass the applied voltage from the pin to the internal node, thereby forcing the voltage at the internal node to the desired level.
29. The method of claim 28, further comprising using a pass control circuit to drive the pass circuit.

PENDING CLAIMS

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30. The method of claim 28, wherein the pass control circuit comprises an n-channel MOS transistor having a drain coupled to the internal node, the n-channel MOS transistor configured to, when turned on, pass the voltage at the internal node to a source of the n-channel MOS transistor and to the pass circuit.
31. The method of claim 28, further comprising providing an oscillating control signal to the pass circuit.
32. The method of claim 31, further comprising using a ring oscillator to provide the oscillating control signal to the pass circuit.
- D1*
33. The method of claim 28, wherein the pass circuit comprises:  
a pass gate having first, second, and third terminals, the first terminal coupled to a pass control circuit, the second terminal coupled to the internal node, the third terminal coupled to the pin; and  
a capacitor coupled between the first terminal of the pass gate and the pass control circuit such that a voltage at the first terminal of the pass gate is driven to cause a voltage at the second terminal voltage to be passed to the third terminal for reading the voltage at the internal node.
34. The method of claim 33, wherein the pass gate comprises an n-channel MOS transistor.
35. A method comprising:  
receiving a read signal;  
coupling a pass circuit between an internal node and a pin of an integrated circuit;  
resetting the pass circuit with a reset circuit based on a first state of the read signal; and  
passing the voltage from the internal node to the pin based on a second state of the read signal.
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- could include*
36. The method of claim 35, wherein passing the voltage from the internal node includes driving a control node connected to the pass circuit to a first voltage based on the second state of the read signal.
37. The method of claim 36, wherein driving includes passing an oscillating signal to the pass circuit.
38. The method of claim 36, wherein resetting the pass circuit includes driving the control node to a second voltage based on the first state of the read signal.
39. The method of claim 38, wherein resetting the pass circuit includes driving the control node to ground.
- D*
40. A method comprising:  
receiving a read signal;  
coupling a pass circuit between an internal node and a pin of an integrated circuit;  
applying an applied voltage to the pin;  
resetting the pass circuit with a reset circuit based on a first state of the read signal; and  
passing the applied voltage from the pin to the internal node based a second state of the read signal.
41. The method of claim 40, wherein passing the applied voltage from the pin includes driving a control node connected to the pass circuit to a first voltage based on the second state of the read signal.
42. The method of claim 41, wherein driving includes passing an oscillating signal to the pass circuit.

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43. The method of claim 41, wherein resetting the pass circuit includes driving the control node to a second voltage based on the first state of the read signal.
44. The method of claim 43, wherein resetting the pass circuit includes driving the control node to ground.
45. (Amended) A method comprising:  
receiving a read signal;  
passing a voltage between an internal node and an access pin based on a first signal level of the read signal; and  
isolating the access pin from the internal node based on a second signal level of the read signal.
- D*
46. The method of claim 45, wherein passing a voltage includes pulling a control voltage of a control node to a first voltage level based on the first signal level of the read signal.
47. The method of claim 46, wherein isolating the access pin includes pulling a control voltage of a control node to a second voltage level based on the second signal level of the read signal.
48. The method of claim 45, wherein passing a voltage includes:  
activating a control device connecting between the internal node and a pass node; and  
activating a pass device connecting between the pass node and the access pin.
49. The method of claim 48, wherein isolating the access pin includes deactivating the pass device.

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50. The method of claim 49, wherein isolating the access pin includes deactivating the control device.
51. The method of claim 50, wherein isolating the access pin includes connecting the pass node to ground.
52. The method of claim 45, wherein isolating the access pin includes disabling a pass circuit connected between the access pin and the internal node.
53. The method of claim 45, wherein isolating the access pin includes disconnecting a pass circuit connected to the access pin from a pass control circuit connected to the internal node.
- Q*
54. The method of claim 45, wherein isolating the access pin includes disconnecting a first terminal of a pass device connected to the access pin from a second terminal of the pass device connected to the internal node.
55. The method of claim 45, wherein isolating the access pin includes cutting off a conduction channel between a source of a pass transistor connected to the access pin and a drain of the pass transistor.
56. A method comprising:  
receiving a read signal;  
passing an internal voltage from an internal node to an access pin based on a first signal level of the read signal; and  
isolating the access pin from the internal node based on a second signal level of the read signal.

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from 61*
57. The method of claim 56, wherein passing an internal voltage includes:  
passing the internal voltage to a pass node; and  
passing the internal voltage from the pass node to the access pin.
58. The method of claim 57, wherein:  
passing the internal voltage to a pass node is performed by a pass control circuit  
connecting between the internal node and the pass node; and  
passing the internal voltage from the pass node to the access is performed by a pass  
circuit connecting between the pass node and the access pin.
- D1*
59. The method of claim 57, wherein isolating the access pin includes pulling a voltage of the  
pass node to ground.
60. The method of claim 56, wherein passing an internal voltage includes:  
activating a control device connecting between the internal node and a pass node; and  
activating a pass device connecting between the pass node and the access pin.
61. The method of claim 60, wherein isolating the access pin includes deactivating the pass  
device.
62. The method of claim 61, wherein isolating the access pin includes deactivating the  
control device.
63. The method of claim 62, wherein isolating the access pin includes connecting the pass  
node to ground.

- Control bus (1)*
64. A method comprising:  
receiving a read signal;  
passing a pin voltage from an access pin to an internal node based on a first signal level of the read signal; and  
isolating the access pin from the internal node based on a second signal level of the read signal.
- D*
65. The method of claim 64, wherein passing a pin voltage includes:  
turning on a control transistor connecting between the internal node and a pass node; and  
turning on a pass transistor connecting between the pass node and the access pin.
66. The method of claim 65, wherein isolating the access pin includes turning off the pass transistor.
67. The method of claim 66, wherein isolating the access pin includes turning off the control transistor.
68. The method of claim 67, wherein isolating the access pin includes connecting the pass node to ground.
69. A method comprising:  
receiving a read signal;  
activating a control device during a first signal level of the read signal to pass a voltage between an internal node inside a memory device and a pass node inside the memory device;  
activating a pass device during the first signal level of the read signal to pass the voltage between the pass node and an input/output pin of the memory device;  
deactivating a reset circuit during the first signal level of the read signal to isolate the pass



*Somebody*  
node from ground;

deactivating the control device during a second signal level of the read signal;

deactivating the pass device during the second signal level of the read signal; and

activating the reset circuit during the second signal level of the read signal to connect the pass node to ground.

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70. The method of claim 69, wherein activating a control device during a first signal level of the read signal to pass a voltage between an internal node inside a memory device and a pass node inside the memory device includes:

passing an internal voltage from the internal node to the pass node.

*Somebody*  
71. The method of claim 70, wherein activating a pass device during the first signal level of the read signal to pass the voltage between the pass node and an input/output pin of the memory device includes:

passing the internal voltage from the pass node to the input/output pin.

72. The method of claim 71, wherein activating a control device during a first signal level of the read signal to pass a voltage between an internal node inside a memory device and a pass node inside the memory device includes:

passing an applied voltage from the pass node to the internal node.

73. The method of claim 72, wherein activating a pass device during the first signal level of the read signal to pass the voltage between the pass node and an input/output pin of the memory device includes:

passing the applied voltage from the input/output pin to the pass node.